IN THE SPECIFICATION:

Please revise the specification as follows:

Please amend the paragraph starting on page 2, line 16 as follows:

A1

In the system of Figure 1A, the master device 24 transmits data on the bus 36 contemporaneously with clock signals on the clock-from-master path 30. In other words, the transmission of data from the master device 24 to the slave devices 26 is timed by the clock signals on the clock-from-master path 30. Conversely, each slave device transmits data contemporaneously with the clock signal on the clock-to-master path 28. That is, the transmission of data from the slave devices 26 to the master device 24 is timed by the clock signals on the clock-to-master path 28. The scheme of having clock and data signals travel in the same direction is used to reduce clock data skew.

Please amend the paragraph starting on page 2, line 25 as follows:

A2

Figure 1B illustrates timing circuitry used to coordinate the transmission and receipt of signals within a prior art slave device 26. As shown, complementary clock signals CTM and $\overline{CTM}$ ~~CTM'~~, respectively on lines 28A and 28B, are received at a differential input buffer 32, the output of which is applied to the reference and phase offset inputs of a Delay-Locked Loop (DLL) 33 to generate an internal transmit clock signal on line 34. Similarly, complementary clock signals CFM and $\overline{CFM}$ ~~CFM'~~, respectively on lines 30A and 30B, are received at a differential input buffer 35, the output of which is applied to the reference and phase inputs of a DLL 36 to generate an internal receive clock signal on line 37. This differential buffering scheme is different than the non-differential (single-ended) buffering scheme used for data reception. Thus, prior art slave devices using this configuration are susceptible to timing skew errors between the frequency signal and the data signal.

Please amend the paragraph starting on page 8, line 8 as follows:

A3 Cont'd

Figure 4 also illustrates that the circuit 70 includes a divide-by-N circuit 104 to divide down the clock signal from the clock source 100. The divide-by-N circuit 104 produces a lower frequency phase signal that will not produce standing waves on the phase line 78. The divide-by-N circuit may produce a ~~non-~~ fractional number (e.g., 3.5). Thus, the divide-by-N circuit may be viewed as an M/N divider, where M and N are each integers.

Please amend the paragraph starting on page 9, line 6 as follows:

Effective frequency can be explained with reference to Figure 5B. Pseudo random number generator 110A consists of ~~4 linear feedback shift registers~~ four flip-flops 701-704 ~~(hereinafter LFSRs)~~ that together form a linear feedback shift register (LFSR), and an exclusive-OR (XOR) gate 700, with inputs from the flip-flops ~~LFSR~~ 703 and ~~LFSR~~ 704 and an output to the ~~LFSR~~ flip-flop 701. The XOR gate 700 produces a digital high output when the outputs of flip-flops 703 and 704 are opposite, otherwise a digital low output signal is produced, this results in the following pattern at the output of flip-flop 701: 100010011010111, as shown in Figure 5B. Thus, even with a periodic input clock signal, CLK, the output of the pseudo random number generator 110A is not periodic. The output signal provides only phase information, not clock information. Thus, it has an effective frequency, but is not periodic.

A4

Please amend the paragraph starting on page 9, line 16 as follows:

For the circuit 110A of Figure 5B, the number of ~~registers~~ flip-flops/bits is preferably less than N, where N is the maximum number of clock cycles that can transpire without a transition of the phase reference without the loss of phase lock. The LFSR must have a transition at least once every K clock cycles, where K is the number of ~~registers~~ flip-flops in the LFSR. Naturally, other circuits may be used to implement a pseudo-random number generator, as appreciated with reference to Figures 5C and 5D.

A5